TITLE OF THE INVENTION

VIDEO REPRODUCING APPARATUS AND METHOD AND APPARATUS AND METHOD FOR ADJUSTING HORIZONTAL SYNCHRONOUS SIGNAL

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority of Korean Patent Application No. 2002-76526, filed on December 4, 2002, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to a video signal reproducing apparatus, and more particularly, to a video signal reproducing apparatus and method, including an apparatus and method for adjusting a horizontal synchronous signal.

2. Description of the Related Art

[0003] FIG. 1 is a schematic block diagram of a conventional video signal reproducing apparatus. The conventional video signal reproducing apparatus includes an analog-to-digital converter (ADC) 100, a phase locked loop (PLL) circuit 110, a line buffer 120, a timing control logic 130, and a scaler 140.

[0004] The ADC 100 converts an input analog video signal into a digital video signal.

[0005] The PLL circuit 110 receives an input horizontal synchronous signal H_sync, and produces a video clock Video_Clock and a clock signal DCLK.

[0006] The line buffer 120 stores a display line of a digital video signal (RGB signal) in a unit of a display line. The line buffer 120 has a smaller memory capacity than a frame buffer, which can accommodate all the data displayed on a screen.

[0007] The timing control logic 130 controls writing to and reading from the line buffer 120, stores an output resolution, and outputs the video clock Video_Clock_out, a horizontal synchronous signal H_sync_out, and a vertical synchronous signal V-sync_out, for reproducing video.

[0008] The scaler 140 converts the digital video signal stored in the line buffer 120, into a video signal with a resolution suitable for reproduction and then outputs the video signal having the converted resolution.

[0009] In the video signal reproducing apparatus shown in FIG. 1, the input video signal is temporarily stored in the line buffer 120 so a calculation operation can be performed to convert the input video signal into a video signal having a resolution suitable for a display device and allow for buffering of data due to the different speeds of inputting and outputting the video signal. The input speed of the input video signal and the recording speed of the input video signal in the line buffer 120 are set by a user, but may vary according to the condition of the source used for reproducing the input video signal. However, the video signal output from the video signal reproducing apparatus has a fixed period depending on the characteristics of the display device. Thus, as writing and reading operations in the line buffer 120 are repeated, the timing of writing data to the line buffer 120 may outpace the timing of reading data from the line buffer 120.

[0010] In order to solve this problem, various control signals input to the line buffer 120 are reset right after the output vertical synchronous signal V_sync_out is generated to keep a predetermined timing between the write operation and the read operation in the line buffer 120, i.e., input and output timing periods of the video signal.

[0011] However, such a reset based on the output vertical synchronous signal may affect a period of the output horizontal synchronous signal H_sync_out. There are as many output horizontal synchronous signals as horizontal lines of a frame in a period of the output vertical synchronous signal. If resetting is performed immediately after the output vertical synchronous signal is generated, the point in time when the output horizontal synchronous signal is generated may be, at maximum, two periods slower than the point in time when the previous output horizontal synchronous signal was generated. FIG. 2 illustrates an output horizontal synchronous signal, which is delayed according to a reset signal being applied immediately after an output vertical synchronous signal is produced.

[0012] In addition, when a period of an output horizontal synchronous signal falls outside an allowed period of a horizontal synchronous signal required by the display device, an undesirable phenomenon such as bouncing, rolling, or the like may occur during display of the video signal.

SUMMARY OF THE INVENTION

[0013] The present invention provides a video signal reproducing apparatus and method, including an apparatus and method for adjusting an output horizontal synchronous signal by measuring a period of the output horizontal synchronous signal and adjusting a period of the horizontal synchronous signal to a desirable period.

[0014] Additional aspects and/or advantages of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

[0015] To achieve the above and/or other aspects and advantages of the present invention, there is provided a video signal reproducing apparatus, which transforms a format of an input video signal, generates horizontal and vertical synchronous signals, and displays the transformed video signal, including a measurer measuring a period of the horizontal synchronous signal, a comparator comparing the measured period of the horizontal synchronous signal with a predetermined reference range, and an adjustor adjusting a period of a clock signal, for producing the horizontal synchronous signal, if the measured period of the horizontal synchronous signal fails to fall within the predetermined reference range.

[0016] If the measured period of the horizontal synchronous signal is above the predetermined reference range, the adjustor may reduce the period of the clock signal and reproduce the horizontal synchronous signal using the reduced clock signal period. Alternatively, if the measured period of the horizontal synchronous signal is under the predetermined reference range, the adjustor may increase the period of the clock signal and reproduce the horizontal synchronous signal using the increased clock signal period.

[0017] To achieve to above and/or other aspects and advantages of the present invention, there is provided a video signal reproducing apparatus, including a converter converting an input analog video signal into a digital video signal, a line buffer storing a display line of the digital video signal, a scaler transforming a format of the digital video signal and then outputting the transformed digital video signal, a controller controlling timing of an inputting the digital video signal into the line buffer and timing of outputting the display line of the digital video signal from the line buffer to the scaler, and producing horizontal and vertical synchronous signals, and a horizontal synchronous signal detector measuring a period of the horizontal synchronous signal, adjusting a period of a clock signal for producing a new horizontal synchronous signal according

to the measured period, and providing the controller with the adjusted period of the clock signal, wherein the controller produces the new horizontal synchronous signal using the adjusted clock signal.

[0018] The horizontal synchronous signal detector may include a measurer measuring the period of the horizontal synchronous signal, a comparator comparing the measured period of the horizontal synchronous signal with a predetermined reference range, and an adjustor adjusting the period of the clock signal for producing the new horizontal synchronous signal, if the measured period of the horizontal synchronous signal fails to fall within the predetermined reference range.

[0019] To achieve the above and/or other aspects or advantages of the present invention, there is provided a method of reproducing a video signal, including measuring a period of a horizontal synchronous signal, comparing the measured period with a predetermined reference range; and adjusting a period of a clock signal for producing the horizontal synchronous signal to reproduce a new horizontal synchronous signal if the measured period of the horizontal synchronous signal fails to fall within the predetermined reference range.

[0020] To achieve the above and/or other aspects or advantages of the present invention, there is provided a horizontal synchronous signal adjusting apparatus for a video signal reproducing apparatus that generates horizontal and vertical synchronous signals and displays a corresponding video signal, including a measurer measuring a period of a horizontal synchronous signal, a comparator comparing the measured period of the horizontal synchronous signal with a predetermined reference range, and an adjustor adjusting a period of a clock signal, used to generate horizontal synchronous signals by the video signal reproducing apparatus, if the measured period of the horizontal synchronous signal fails to fall within the predetermined reference range.

[0021] To achieve the above and/or other aspects or advantages of the present invention, there is provided a method of reproducing a video signal, including measuring a period of a horizontal synchronous signal, comparing the measured period with a predetermined reference range, and adjusting a period of a clock signal for producing the horizontal synchronous signal to reproduce a new horizontal synchronous signal, if the measured period of the horizontal synchronous signal fails to fall within the predetermined reference range, and to prevent a reversal of write and read timings of a display line buffer of a corresponding video reproducing apparatus.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] These and/or other aspects and advantages of the present invention will become apparent and more readily appreciated from the following description of the embodiments, taken in conjunction with the accompanying drawings of which:

FIG. 1 is a schematic block diagram of a conventional video signal reproducing apparatus;

FIG. 2 illustrates an output horizontal synchronous signal delayed according to a reset signal being applied immediately after an output vertical synchronous signal is produced;

FIG. 3A is a block diagram of the video signal reproducing apparatus for adjusting a horizontal synchronous signal, according to an embodiment of the present invention;

FIG. 3B is a detailed block diagram of a horizontal synchronous signal detector shown in FIG. 3A; and

FIG. 4 is a flowchart of a method of adjusting a horizontal synchronous signal in the video signal reproducing apparatus shown in FIG. 3A, according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0023] Reference will now be made in detail to the embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below to explain the present invention by referring to the figures.

[0024] FIG. 3A is a block diagram of a video signal reproducing apparatus for adjusting a horizontal synchronous signal, according to an embodiment of the present invention. Referring to FIG. 3A, the video signal reproducing apparatus includes at least a converter 300, a line buffer 310, a scaler 320, a controller 330, a horizontal synchronous signal detector 340, and a PLL circuit 350.

[0025] The converter 300 converts an input analog video signal (RGB signal) into a digital video signal. The clock signal from the PLL circuit 350 is used for the converting operation.

[0026] The line buffer 310 stores the digital video signal output from the converter 300. More specifically, the line buffer 310 writes the digital video signal therein according to a write control signal and outputs the digital video signal according to a read control signal. Writing to the line

buffer 310 is generally performed after data is read from the line buffer 310. However, since the read timing is fixed and the write timing is variable, it is necessary to keep a predetermined distance between the write and read timings so that the write and read timings are not reversed.

[0027] The scaler 320 transforms the format (resolution) of the digital video signal read (output) from the line buffer 310, into a format suitable for a current display device.

[0028] The controller 330 provides the line buffer 310 with the write and read control signals to control input to and output from the line buffer 310. The controller 330 generates a clock signal and produces horizontal and vertical synchronous signals suitable for the current display device using the clock signal. The controller 330 generates a reset signal immediately after producing the vertical synchronous signal to keep a predetermined distance between read and write timings of the line buffer 310. With the generation of the reset signal, the controller 330 starts counting until the horizontal synchronous signal is produced. As a result, the interval between the previous horizontal synchronous signal and the horizontal synchronous signal produced after the reset is added to the period of the horizontal synchronous signal, thereby increasing the period by $+\alpha$.

[0029] The horizontal synchronous signal detector 340 measures the period of the horizontal synchronous signal output from the controller 330, and based on the measurement result, adjusts the frequency (or period) of a predetermined clock signal necessary for producing the horizontal synchronous signal. Next, the horizontal synchronous signal detector 340 provides the controller 330 with the adjusted clock signal. The controller 330 uses the adjusted clock signal to compensate for $+\alpha$ by moving up the point of time when the horizontal synchronous signal will be generated.

[0030] FIG. 3B is a block diagram of the horizontal synchronous signal detector 340. Referring to FIG. 3B, the horizontal synchronous signal detector 340 includes at least a measurer 341, a comparator 342, and an adjuster 343.

[0031] The measurer 341 measures the period of the horizontal synchronous signal output from the controller 330.

[0032] The comparator 342 compares the period of the horizontal synchronous signal, measured by the measurer 341, to a predetermined reference range and then determines whether the period of the horizontal synchronous signal falls within the predetermined reference range.

[0033] If the period of the horizontal synchronous signal does not fall within the predetermined reference range, the adjustor 343 adjusts the period of the clock signal range for producing the horizontal synchronous signal, and then provides the controller 330 with the adjusted clock signal. The controller 330 reproduces a new horizontal synchronous signal based on the adjusted clock signal. In other words, the adjustor 343 reduces the period of the clock signal when the measured period of the horizontal synchronous signal is above the predetermined reference range, and then provides the controller 330 with the clock signal having the reduced period. As a result, the controller 330 can produce and output a new horizontal synchronous signal which has a shorter period, whereby an occurrence time of the horizontal synchronous signal is moved up. In contrast, if the measured period of the horizontal synchronous signal is under the predetermined reference range, the adjustor 343 increases the period of the clock signal. When the clock signal having the increased period is provided to the controller 330, the controller 330 reproduces a new horizontal synchronous signal which has a longer period, whereby an occurrence time of the horizontal synchronous signal is delayed.

[0034] FIG. 4 is a flowchart of a method of adjusting a horizontal synchronous signal in the video signal reproducing apparatus shown in FIG. 3A. In operation 400, the period of the horizontal synchronous signal, output from the controller 330, is measured.

[0035] In operation 410, the measured period is compared to the predetermined reference range.

[0036] If the measured period of the horizontal synchronous signal is above the predetermined reference range, then in operation 420, the period of the clock signal for producing the horizontal synchronous signal is reduced. In operation 430, a horizontal synchronous signal having a shorter period is reproduced based on the reduced period of the clock signal.

[0037] In operation 440, if the measured period of the horizontal synchronous signal is under the predetermined reference range, then in operation 450, the period of the clock signal is increased. Subsequently, in operation 460, a horizontal synchronous signal having a longer period is reproduced based on the increased period of the clock signal.

[0038] Alternatively, if the measured period of the horizontal synchronous signal falls within the predetermined reference range the horizontal synchronous signal is output as is, without an adjustment, in operation 470.

[0039] Thus, as noted above, in order to stabilize input and output operations of a line buffer, a reset signal is generated based on a vertical synchronous signal. However, the reset signal affects the occurrence timing of a horizontal synchronous signal. Accordingly, in embodiments of the present invention, by detecting and adjusting the period of the horizontal synchronous signal to fall within a predetermined range, errors, caused by a change in the horizontal synchronous signal, and observed on the screen of a display device, can be prevented.

[0040] Although a few embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes may be made in this embodiment without departing from the principles and spirit of the invention, the scope of which is defined in the claims and their equivalents.